Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) An apparatus, comprising:

(a) a single die;

(b) a first circuitry disposed on said single die including:

a deserializer for converting at least one serial differential bit stream into a character stream;

a decoder receiving said character stream to form a decoded data stream; and

a means for aggregating said decoded data stream and reconstructing a parallel word according to a desired protocol definition;

(c) a second circuitry disposed on said single die including:

a means for presenting a second parallel word according to said desired protocol definition to form an altered data stream,

an encoder receiving said altered data stream to form an encoded data stream;

a serializer for converting said encoded data stream into said at least one serial differential bit stream, wherein said first circuitry and said second circuitry are capable of implementing at least two interconnect protocol definitions, said at least two interconnect protocol definitions including a single-thread, multiple-speed protocol method and a multiple-thread, single-speed protocol method.

2. (Canceled)

3. (Previously Presented) The apparatus as claimed in claim 1, wherein at least two interconnect protocol definitions include a 10 Gigabit Fibre Channel protocol definition and a 4 Gigabit, 2 Gigabit, 1 Gigabit Fibre Channel protocol definition.

4. (Currently Amended) A method, executed by a communication device, for converting a serial bit stream to a word, comprising:

(a) converting a at least one serial data stream to a character stream;

(b) decoding of said character stream to form a decoded data stream; and

(c) aggregating said decoded data stream according to a desired interconnect protocol definition; wherein circuitry disposed on a single die is capable of transforming at least one serial bit stream into a word in accordance with at least two interconnect protocol definitions, said at least two interconnect protocol definitions including a single-thread, multiple-speed protocol method and a multiple-thread, single-speed protocol method.

5. (Canceled)

6. (Previously Presented) The method as claimed in claim 4, wherein said at least two interconnect protocol definitions include a 10 Gigabit Fibre Channel protocol definition and a 4 Gigabit, 2 Gigabit, 1 Gigabit Fibre Channel protocol definition.

7. (Original) The method as claimed in claim 6, wherein decoding of said at least one serial data streams converts 10 bits of data to 8 bits of data.

8. (Original) The method as claimed in claim 6, wherein aggregating of said decoded data stream aligns said decoded data stream to reconstruct said parallel data word according to said desired interconnect protocol definition.

9. (Currently Amended) A method, executed by a communication device, for converting a word to a serial bit stream, comprising:

(a) selecting a word stream for transmission;

(b) presenting said word stream according to a desired interconnect protocol definition to form an altered data stream;

(c) encoding said altered data stream to form an encoded data stream; and

(d) converting said encoded data stream to at least one serial differential bit stream; wherein circuitry disposed on a single die is capable of transforming said word stream into at least one serial differential bit stream in accordance with at least two interconnect protocol definitions, said at least two interconnect protocol definitions including a single-thread, multiple-speed protocol method and a multiple-thread, single-speed protocol method.

10. (Canceled)

11. (Previously Presented) The method as claimed in claim 9, wherein said at least two interconnect protocol definitions are a 10 Gigabit Fibre Channel protocol definition and a 4 Gigabit, 2 Gigabit, 1 Gigabit Fibre Channel protocol definition.

12. (Original) The method as claimed in claim 11, wherein encoding of said altered data stream converts 8 bits of data to 10 bits of data.

13. (Previously Presented) An apparatus, comprising:

(a) a single die;

(b) means for transforming at least one serial differential bit stream into a parallel word; said transforming means being disposed on said single die; means for converting a second parallel word into at least one serial differential bit stream; said converting means being disposed on said single die; said converting means including an input selector in which said apparatus operates according to a selected protocol definition; wherein said transforming means and said converting means are capable of implementing at least two interconnect protocol definitions, said at least two interconnect protocol definitions including a single-thread, multiple-speed protocol method, a multiple-thread, single-speed protocol method and a multiple-thread, multiple-speed protocol method.

14. (Canceled)

15. (Previously Presented) The apparatus as claimed in claim 13, wherein at least two interconnect protocol definitions include a 10 Gigabit Fibre Channel protocol definition and a 4 Gigabit, 2 Gigabit, 1 Gigabit Fibre Channel protocol definition.

16. (Original) The apparatus as claimed in claim 13, wherein said transforming means includes a deserializer, a decoder, and an aggregator capable of implementing at least two interconnect protocol definitions.

17. (Original) The apparatus as claimed in claim 13, wherein said converting means includes a data presenter, an encoder, and a serializer capable of implementing at least two interconnect protocol definitions.

18. (Previously Presented) The apparatus as claimed in claim 1, wherein said at least two interconnect protocol definitions further includes a multiple-thread, multiple-speed protocol method.

19. (Previously Presented) The method as claimed in claim 4, wherein said at least two interconnect protocol definitions further includes a multiple-thread, multiple-speed protocol method.

20. (Previously Presented) The method as claimed in claim 9, wherein said at least two interconnect protocol definitions further includes a multiple-thread, multiple-speed protocol method.

21. (Previously Presented) The apparatus as claimed in claim 13, wherein said at least two interconnect protocol definitions further includes a multiple-thread, multiple-speed protocol method.